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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,396	09/27/2006	Ryosuke Meshii	P30769	8147

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EXAMINER	
KUSUMAKAR, KAREN M	
ART UNIT	PAPER NUMBER
2829	

NOTIFICATION DATE	DELIVERY MODE
11/18/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
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Office Action Summary	Application No.	Applicant(s)	
	10/599,396	MESHII ET AL.	
	Examiner	Art Unit	
	KAREN M. KUSUMAKAR	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. As of the amendment filed 7/28/08, no claims have been added or canceled, and claims 1-11 have been amended. Therefore, claims 1-11 remain pending, with claims 1, 5, and 9 being independent.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masakazu (JP Hei 10-090300, Applicant's admitted prior art) in view of Keichi et al (JP Hei 6-340452, Applicant's admitted prior art).

3. As to claims 1-2 and 5-6, Masakazu discloses

a method for manufacturing a semiconductor physical quantity sensor of electrostatic capacitance type (page 2, line 21-page 3, line 9 and Fig. 9 of the present application) **in which mutually facing peripheral areas (referred to as bonding areas) of an insulating substrate and a semiconductor substrate are contacted for anodic bonding** (5, Fig. 9 of the present application)**, while both substrates have an**

anodic bonding voltage applied therebetween so as to be integrated by anodic bonding (11, Fig. 9 of the present application)**, with a fixed electrode** (7, Fig. 9 of the present application) **being formed on a bonding face-side surface of the insulating substrate** (2, Fig. 9 of the present application)**, and with a movable electrode** (4, Fig. 9 of the present application) **being formed on a bonding face-side surface of the semiconductor substrate** (1, Fig. 9 of the present application)**, the method comprising: a first step of forming, before the anodic bonding, an equipotential wiring to short-circuit the fixed electrode to the movable electrode on the bonding face-side surface of the insulating substrate/semiconductor substrate inside the bonding area** (page 2, lines 21-25 and Fig. 9 of the present application)**, and to be prevented from being directly sandwiched between the both substrates** (Fig. 9 of the present application; 7(7c) connects to substrate 1 indirectly, therefore, indirect sandwiched between the both substrates)**; a second step of performing the anodic bonding** (page 3, lines 1-4) **[claims 1 and 5].**

However, Masakazu fails to disclose:

a third step of cutting and removing the equipotential wiring after the anodic bonding [claims 1 and 5];

where the third step, the equipotential wiring is cut by laser irradiation allowed to pass through from the insulating substrate [claims 2 and 6].

Nonetheless, these features are well known in the art and would have been an obvious modification of the method disclosed by Masakazu, as evidenced by Keichi.

Keichi discloses:

a third step of removing the equipotential wiring after the anodic bonding is cut by laser irradiation (page 3, lines 19-25 of the present application)**;**

Given the teaching of Keichi, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying the method disclosed by Masakazu by employing the well known or conventional features of laser irradiation, such as evidenced by Keichi, in order to cut and remove the equipotential wiring that is within the bonding areas via the glass substrate for the purpose of making the movable electrode movable and detecting a pressure, since the equipotential wiring is under the glass substrate and the glass substrate has the property allowing the laser irradiation to pass through .

4. Claims 3-4, 7-8, and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masakazu in view of Keichi as applied to claims 1 and 5, and further in view of Katsumi et al (See attached Machine English Translation of JP Hei 9-196700, Applicant's admitted prior art, and Katsumi hereinafter).

5. As to claims 3-4, 7-8, and 10-11, Masakazu in view of Keichi discloses substantial features of the claimed invention (see paragraph above), and further discloses (see Masakazu):

conductive film layers (9a and 9b, Fig. 9 of the present application) **are exposed at bottom portions of respective through-holes which are provided in the insulating substrate** (8a and 8b, Fig. 9 of the present application) **for the fixed**

electrode (7/7c, Fig. 9 of the present application) **and the movable electrode** (4, Fig. 9 of the present application) **as to cause a current to flow in the equipotential wiring** (70, Fig. 9 of the present application) **[claims 3 and 7].**

However, Masakazu in view of Keichi fails to disclose:

where in the third step, "a voltage is applied" between conductive film layers exposed at bottom portions of respective through-holes which are provided in the insulating substrate for the fixed electrode and the movable electrode so as to cause a current to flow in the equipotential wiring, "and the equipotential wiring is cut by heat generated based thereon" [claims 3 and 7];

where in the first step, the equipotential wiring has reduced width at a cutting location thereof [claims 4, 8, and 10-11].

Nonetheless, these features would have been obvious modification of the method disclosed by Masakazu in view of Keichi, as evidenced by Katsumi.

Katsumi discloses:

a voltage is applied, and the equipotential wiring is cut by heat generated based thereon ([0078], line 1) **[claims 3 and 7];**

where in the first step, the equipotential wiring has reduced width at a cutting location thereof ([0043]-[0044, Drawing 9A) **[claims 4, 8, and 10-11];**

Given the teaching of Katsumi, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Masakazu in view of Keichi by employing the well known or conventional features of voltage generated heat, such as disclosed by Katsumi, in order to cut the

equipotential wiring in the above structure during the third step in a facilitating manner other than cutting with laser irradiation.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masakazu in view of Keichi and Katsumi.

7. As to claim 9, arguments made in paragraphs 8-10 above also apply.

Response to Arguments

2. Applicant's arguments filed 7/28/08 have been fully considered but they are not persuasive. The previous rejection is upheld and reiterated above. Applicant makes the following arguments:

a. Masakazu does not disclose any such forming of equipotential wiring to short circuit the fixed electrode to the movable electrode, therefore modifying Masakazu with Keichi (i.e. cutting the wiring) would not result in the combination of claim 1.

b. Keichi requires exposing connection wiring in advance for the purpose of cutting the wiring by laser, which also requires cutting the glass member. This is not required in claim 1.

c. Keichi cuts the connection wiring and the silicon structure at the same time, so that a high laser power is required. This is not required in claim 1.

d. Mazakazu does not disclose equipotential wiring on the bonding-face side surface of a semiconductor substrate but instead on the glass substrate.

Examiner respectfully disagrees for the following reasons:

a) According to lines 23-25 on page 2 and lines 1 and 3 on page 3 of Applicant's disclosure, the equipotential wiring is formed and both electrodes are electrically connected via the equipotential wiring 70. Therefore, the wiring 70 is existing and can be cut per Keichi.

b) The Keichi reference is used for its teachings of cutting the equipotential wiring. How it is done and at what phase of the process it is done is not a limitation recited in Applicant's claim 1.

c) Again, the Keichi reference is used for its teachings of cutting the equipotential wiring. The type of laser or power of the laser is not a limitation recited in Applicant's claim 1.

d) Examiner is uncertain what the Applicant is trying to say. It is believed the Applicant is arguing that the wiring itself is formed on the semiconductor substrate whereas the prior art has it formed on the glass substrate. Examiner respectfully calls Applicant's attention to claim 5, which recites "forming, before the anodic bonding, an equipotential wiring to short-circuit the fixed electrode to the movable electrode on the bonding face-side of the semiconductor substrate". As best as Examiner can tell, the thing that is on the bonding-face side of the semiconductor substrate is the movable

electrode. Claim 5 does not limit the wiring to the semiconductor substrate. Instead it limits the wiring only to short-circuiting the movable electrode and the fixed electrode. How and where it performs that function is not a limitation of claim 5.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Any response to this Office Action should be faxed to (571) 273-8300 or mailed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Hand-Delivered responses should be brought to:

Customer Service Window

Randolph Building

401 Dulany Street

Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAREN M. KUSUMAKAR whose telephone number is (571) 270-3520. The examiner can normally be reached on Mon - Thurs 7:30a - 5:00p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. M. K./
Examiner, Art Unit 2829
11/9/2008

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829